REMARKS

Claims 1-8 are pending. Claims 6-8 are withdrawn from consideration.

It is believed that this Amendment is fully responsive to the Office Action dated **December 19, 2001**.

Rejection Under 35 U.S.C. §102:

Claim 1 is rejected under 35 U.S.C. §102(b) as being anticipated by **Yamashita et al. (U.S. Patent No. 5,610,430)**.

> "Yamashita et al. discloses (see fig. 1-3 and col. 11, lines 36-52) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 31 by a substrate isolation insulating film (unnumbered), provided with a T-shaped gate electrode 13 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) and having a thickness of the gate insulating film 12 directly under the crosspiece-shaped conductor pattern greater than the thickness of the gate insulating film directly under the main gate electrode."

The Applicant respectfully disagrees with the Office position. According to a semiconductor device of the cited reference Yamashita et al., a semiconductor layer 15 serving as an active region is not isolated from a semiconductor substrate 11, and therefore, the above semiconductor device is not an insulated gate type (i.e., SOI type) semiconductor device.

Also, a T-shaped gate electrode 13 as shown in Yamashita et al. is extended toward the vertical direction with respect to the semiconductor substrate 11, while the T-shaped gate electrode in the present invention extends in parallel with respect to the semiconductor substrate.

Independent claim 1, as amended, has positively stated that:

> "1. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, provided with a T-shaped gate electrode comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode and having a length larger than the width of source and drain regions, and having a thickness of the gate insulating film formed directly under the entire region of the crosspiece-shaped conductor pattern greater than the thickness of the gate insulating film directly under the main gate electrode."

Therefore, the semiconductor device according to the present invention defined in claim 1, fundamentally differs from Yamashita et al.

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 1, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 1 patentably distinguishes Yamashita. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 2 is rejected under 35 U.S.C. §102(b) as being anticipated by **Imai et al. (JP 8-125187)**.

In rejecting the claimed invention, the outstanding Office action has positively stated that:

> "Han et al. discloses (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 16 serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film 15, wherein a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region 9 positioned at an interface between that first conductivity type body contact region 8 and a second conductivity type source 6 and drain 7 regions is made greater than the thickness of a gate insulating film directly under the main gate electrode 5."

Even though the body of the explanation specifies Han et al., it is taken that the Office meant Imai et al. The Applicant respectfully disagrees with the Office position. The cited reference Imai et al. discloses a SOI type semiconductor device provided with a T-shaped gate electrode 5. Further, the above-device has a thickness of a gate insulating film 18 formed directly under a part of the crosspiece-shaped conductor pattern abutting on the T-shaped gate electrode 5, i.e., on a part of a body contact region 8 (that is, in the region 17 mentioned in the above item (1)), which thickness is greater than that of the gate insulating film 4 formed directly under the trunk-shaped main gate electrode of the T-shaped gate electrode 5.

In this connection, please note that reference numerals 6, 7, 9, and 12 denote a source region, drain region, channel region, and a body contact electrode, respectively.

According to Imai et al., the gate insulating film 18 having the above greater thickness is formed on a part of the body contact region 8. Further, a part of the T-shaped gate electrode 5 is provided on the above part of the body contact region 8 (i.e., in the above-mentioned region 17).

In contradistinction, the present invention defined in claim 2 a thickness of an insulating film provided on a surface of a semiconductor region which is located at an interface between the body contact region and both source and drain regions, the surface is made greater than the thickness of a gate insulating film formed directly under a gate electrode.

Further, the present invention defined in claim 2 that the above gate electrode is not located on the body contact region.

Thus, according to the present invention as defined in clam 2, it is possible to eliminate the parasitic capacitance derived from the crosspiece-shaped conductor pattern of the gate electrode (i.e., separator), by removing the above separator.

Also, according to the present invention as defined in claim 2, it is not necessary to take the change in the performance of the transistor derived from the current flowing between source and drain regions via the channel region under the separator, at the junction portion between the separator and the main gate electrode into consideration.

Independent claim 2, as amended, has positively stated that:

> "2. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region and a second conductivity type source and drain regions is made greater than the

thickness of a gate insulating film directly under a gate electrode, said gate electrode being provided on the region except for said body contact region."

Therefore, the semiconductor device according to the present invention defined in claim 2, completely differs from Imai et al.

It is well settled that:

"A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 2, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 2 patentably distinguishes Yamashita. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 3 is rejected under 35 U.S.C. §102(b) as being anticipated by Imai et al. **(JP 8-125187)**.

In rejecting the claimed invention, the outstanding Office action has positively stated that:

> "Han et al. discloses (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 16 serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film 15, wherein a buried insulating film 18 thicker than the thickness of the gate insulating film directly under a gate electrode 5 is provided on a surface of a first conductivity type semiconductor region 9 positioned at an interface between that first conductivity type body contact region 8 and a second conductivity type source 6 and drain 7 regions."

Even though the body of the explanation specifies Han, it is taken that the Office meant Imai. The Applicant respectfully disagrees with the Office position. The above argument as to claim 2 also applies to claim 3, except that the insulating film having the above greater thickness of claim 2 is replaced, in claim 3, by a buried insulating film. Therefore, the same argument made in the response as applied to claim 2 is incorporated herein by reference and not redundantly recited.

Independent claim 3, as amended, has positively stated that:

> "3. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a buried insulating film thicker than the thickness of the gate insulating film directly under a gate electrode is provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region and a second conductivity type source and drain regions, said gate electrode being provided on the region except for said body contact region."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 3, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in

the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 3 patentably distinguishes Yamashita. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 4 is rejected under 35 U.S.C. §102(b) as being anticipated by **Kawanaka (U.S. Patent No. 5,973,364)**.

In rejecting the claimed invention, the outstanding Office action has positively stated that:

> "Kawanaka discloses (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 316 serving as an active region isolated from a semiconductor substrate 312 by a substrate isolation insulating film 314, wherein a gate electrode of an asymmetric T-shaped conductor pattern is provided and a body contact region 328 and one of a source region 324 and a drain region 326 are isolated through said crosspiece-shaped conductor pattern."

The Applicant respectfully disagrees with the Office position. The cited reference Kawanaka discloses a semiconductor device which is comprised of a semiconductor layer 316 serving as an active region isolated from a semiconductor substrate 312 by a substrate isolation insulating film 314 (i.e., SOI type semiconductor device), wherein a gate electrode 334 of asymmetric T-shape which is comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is used. Thus, a body contact region 328 is separated from both a source region 324 and a drain region 326 by the above gate electrode 334.

However, according to Kawanaka, the above body contact region 328, source region 324 and drain region 326 are electrically independent from others.

In contrast, according to the present invention as defined in claim 4, the body contact region is made the same potential as one of the source region and drain region, and therefore, the body contact region and one of the source region and drain region are short-circuited.

Thus, according to the present invention as defined in claim 4, the following advantage can be obtained. Conventionally, it is necessary to form a contact in the source region, through which contact the source region is connected to the upper metal region thereon. In the present invention of claim 4, however, such contact is not required. Therefore, it becomes possible to narrow the width of the source region. This makes it possible to reduce the size of the source region accordingly.

Therefore, the semiconductor device according to the present invention as defined in clam 4, is completely different from Kawanaka.

Independent claim 4, as amended, has positively stated that:

> "4. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is provided and a body contact region and one of a source region and drain region are isolated through said crosspiece-shaped conductor pattern, said body contact region being made the same potential as one of said source region and drain region."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference."

> *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 4, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 4 patentably distinguishes Yamashita. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 5 is rejected under 35 U.S.C. §102(e) as being anticipated by Yu (U.S. Publication No. 2001/00381123).

In rejecting the claimed invention, the outstanding Office action has positively stated that:

> "Yamashita et al. discloses (see Fig. 1 and page 2, par 0022) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film (unnumbered), wherein a gate electrode of an asymmetric T-shape 46 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode."

Even though the Office cites Yamashita in the body of the rejection based on Yu, it is taken that Yu is intended by the Office. The Applicant respectfully disagrees with the Office position.

According to the semiconductor device of the cited reference Yu, a semiconductor layer (i.e., source and drain regions 22 and 24) serving as an active region is not isolated from a semiconductor substrate 14, and therefore, the above semiconductor device is not an insulated gate type (i.e., SO I type) semiconductor device.

Further, a T-shaped gate electrode 30 as shown in Yu is extended toward the vertical direction with respect to the semiconductor substrate 14. On the other hand, the T-shaped gate electrode in the present invention extends in parallel with respect to the semiconductor substrate.

Therefore, the semiconductor device according to the present invention defined in claim 5, is fundamentally different from Yu.

Independent claim 5, as amended, has positively stated that:

> "5. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern functions as an effective gate electrode."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 5, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number

and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 5 patentably distinguishes Yu. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 5 is rejected under 35 U.S.C. §102(b) as being anticipated by **Yamashita et al. (U.S. Patent No. 5,610,430)**.

In rejecting the claimed invention, the outstanding Office action has positively stated that:

> "Yamashita et al. discloses (see fig. 1-3 and col. 11, lines 36-52) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 31 by a substrate isolation insulating film (unnumbered), wherein a gate electrode of an asymmetric T-shape 13 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode."

The Applicant respectfully disagrees with the Office position. The difference between the present invention and Yamashita et al., is thoroughly and clearly mentioned in the first anticipation rejection as applied to independent clam 1. The arguments in response to the first rejection based on Yamashita is incorporated herein by reference and they are not being redundantly recited herein.

Independent claim 5, as amended, has positively stated that:

> "5. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern functions as an effective gate electrode."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 5, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 5 patentably distinguishes Yamashita. Reconsideration and withdrawal of this rejection are respectfully requested.

Reciprocating Courtesy:

As the Applicant has generously extended the Examiner every courtesy whenever mistakes in the outstanding Office action are found and they are being responded to in good faith. Reciprocating courtesy from the Examiner is respectfully requested whenever similar mistakes, if any, are found in the Applicant's response.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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Enclosures: Version with markings to show changes made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/717,143

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, provided with a T-shaped gate electrode comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode and having a length larger than the width of source and drain regions, and having a thickness of the gate insulating film formed directly under the entire region of the crosspiece-shaped conductor pattern greater than the thickness of the gate insulating film directly under the main gate electrode.

2. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region and a second conductivity type source and drain regions is made greater than the thickness of a gate insulating film directly under a gate electrode, said gate electrode being provided on the region except for said body contact region.

3. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a buried insulating film thicker than the thickness of the gate insulating film directly under a gate electrode is provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region and a second conductivity type source and drain regions, said gate electrode being provided on the region except for said body contact region.

4. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is provided and a body contact region and one of a source region and drain region are isolated through said crosspiece-shaped conductor pattern, said body contact region being made the same potential as one of said source region and drain region.

5. (Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with